Latest Progress in Phase-Change Memory Development for Next-Generation eNVM Targeting 1x & 0x Technology Nodes

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Phase-Change Memory targeting embedded applications (ePCM) has reached a high maturity in advanced technology nodes (e.g., 28 nm and 18 nm), also thanks to Ge-rich GeSbTe (GGST) alloys introduction [1]. Sub-18 nm technology nodes demand for high logic performances, making mandatory the memory integration in the Back-End-Of-Line (BEOL) of the process.
At CEA Leti we are working on next generation of ePCM that should be compliant with BEOL of aggressive technology nodes still ensuring high reliability standards, targeting higher densities required by new applications (i.e., AI ones) [2, 3].

In this work we present some recent developments to enable ePCM in the BEOL of the integration addressing several challenges such as: reliability assessment; programming current reduction; PCM cell scaling; Multi-Level Cell programming (MLC).
Thanks to the introduction of an innovative stack based on GeN underlayer, we show the possibility to reduce the programming current and to tune the active alloy properties, ensuring retention specifications [4] (**Fig. 1**). Then, Carbon implant was introduced to enhance the retention and to reduce the SET state variability. We provide as well demonstration of MLC capability in GGST, tuning the Ge content.
The heater is a key element in a PCM cell, ensuring the proper heating of the active volume. We show first explorations of innovative ALD-based heater alloys targeting the cell scaling (**Fig. 2a**), as well as the integration of innovative dielectrics to surround the PCM cell with the objective to enhance the device thermal efficiency.
Finally, we present possible paths towards a "Vertical Self-Aligned PCM" (VSA-PCM) (**Fig. 2b**) that could enable future 3D implementations addressing high memory densities.

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References

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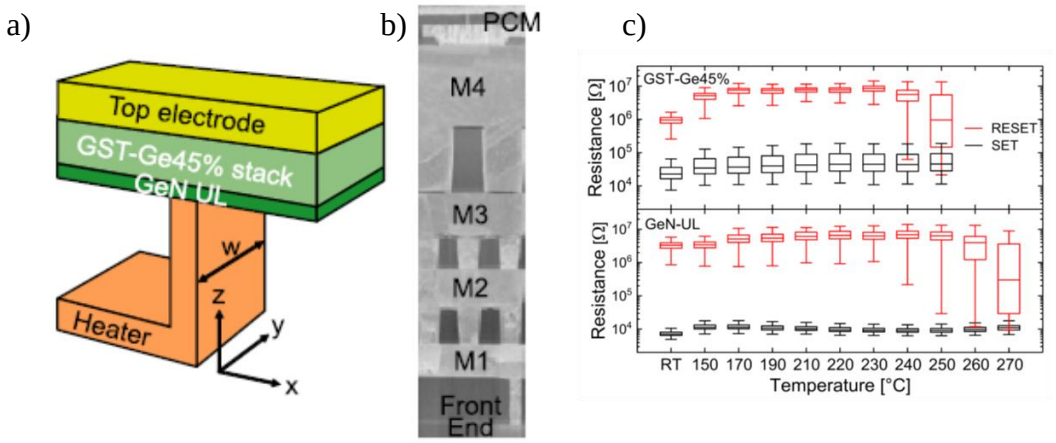

Fig. 1: a) Schematic of a "Wall" PCM based on a GeN Underlayer (UL) and GST-Ge45% compound. The device size is characterized by the heater width (w) (e.g., w = 80 nm). b) TEM image of our PCM device in the BEOL (zx plane). c) Data retention test performed on both SET and RESET states by isochronal annealing of 1 hour at increasing temperatures, highlighting an improvement in GeN-UL, with a RESET state preserved up to 250 °C.

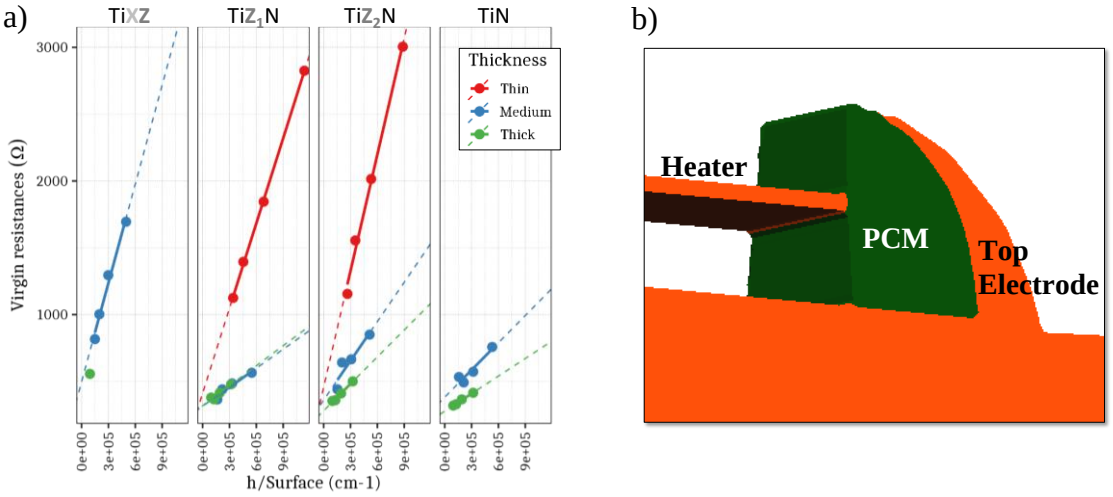

Fig. 2: a) Different Ti-based alloys integrated by ALD in PCM devices for heater resistivity benchmark. Incorporation of element "Z" in TiN (with different Z/Ti ratios) allows higher stability of thinner layers, while replacing N by element "X" in TiZN drastically improves the alloy resistivity. b) Schematic of a "Vertical Self Aligned PCM" (VSA-PCM) enabling possible paths for higher memory densities through 3D integration.